CLAIMS

1-18. (canceled)

19. (currently amended) A circuit for deriving a third order signal from an input signal, the circuit comprising:

input circuitry for providing [[an]] the input signal ~~to the circuit~~ along first, second and third paths,

a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at [[the]] a frequency of the input signal and harmonics thereof, [[and]]

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce [[a]] the third order signal, and

a generator for creating at least one further, different, odd-order signal, each said further, different, odd-order signal being created by combining the input signal with itself.

20. (currently amended) A circuit as claimed in claim 19, for ~~additionally~~ deriving a fifth order signal from [[an]] the input signal, ~~further~~ the generator comprising circuitry for providing the second order signal along a second squared signal path, and a third combiner for combining the second order signal from the second squared signal path with the third order signal to produce [[a]] the fifth order signal.

21. (currently amended) A circuit as claimed in claim 19, for ~~additionally~~ deriving a fifth order signal from [[an]] the input signal, wherein:

the input circuitry provides the input signal along fourth and fifth paths, and

~~further~~ the generator comprises:

a third combiner for combining the input signal from the fourth path with the third order signal to produce a fourth order signal, and

a fourth combiner for combining the input signal from the fifth path with the fourth order signal to produce [[a]] the fifth order signal.

22. (previously presented) A circuit as claimed in claim 19, wherein the input signal is a radio frequency signal.

23. (previously presented) A circuit as claimed in claim 19, further comprising an injector for injecting a direct current signal into at least one of the signal paths.

24. (previously presented) A circuit as claimed in claim 23, wherein the injector is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal.

25. (previously presented) A circuit as claimed in claim 24, further comprising an error corrector arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

26. (previously presented) A circuit as claimed in claim 25, wherein the error corrector is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

27. (currently amended) A circuit as claimed in claim [[23]] 19, further comprising an injector for injecting [[the]] a direct current signal into [[the]] a second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in [[the]] a fifth order signal.

28. (currently amended) A circuit as claimed in claim [[25]] 27, further comprising an error corrector arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

29. (previously presented) A circuit as claimed in claim 19, wherein the combiners are selected from mixers and multipliers.

30. (previously presented) A circuit as claimed in claim 19, wherein the input circuitry comprises at least one splitter for providing the input signal along the signal paths.

31. (previously presented) A circuit as claimed in claim 19, wherein the input circuitry comprises at least one directional coupler for providing the input signal along the signal paths.

32. (currently amended) A polynomial predistorter including a circuit for deriving a third order predistortion signal from an input signal, the circuit comprising:

input circuitry for providing [[an]] the input signal ~~to the circuit~~ along first, second and third paths,

a first combiner for combining the input signal from the first and the second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at [[the]] a frequency of the input signal and harmonics thereof, [[and]]

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce [[a]] the third order signal, and

a generator for creating at least one further, different, odd-order signal, each said further, different, odd-order signal being created by combining the input signal with itself.

33. (currently amended) A method of deriving a third order predistortion signal from an input signal, the method comprising:

providing [[an]] the input signal ~~to a circuit~~ along first, second and third paths,

combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

low-pass filtering the second order signal to remove components at [[the]] a frequency of the input signal and harmonics thereof, [[and]]

combining the filtered second order signal from the squared signal path with the input signal from the third path to produce [[a]] the third order signal, and

creating at least one further, different, odd-order signal, each said further, different, odd-order signal being created by combining the input signal with itself.

34-36. (canceled)

37. (new) A circuit for deriving a third order signal from an input signal, the circuit comprising:

input circuitry for providing the input signal along first, second and third paths,

a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal;

an injector for injecting a direct current signal into at least one of the signal paths, wherein the injector is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal, and

an error corrector arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

38. (new) A circuit as claimed in claim 37, wherein the error corrector is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

39. (new) A circuit for deriving a third order signal from an input signal, the circuit comprising:

input circuitry for providing the input signal along first, second and third paths,

a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal, and

an injector for injecting the direct current signal into the second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in the fifth order signal.

40. (new) A circuit as claimed in claim 39, further comprising an error corrector arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

41. (new) A predistorter for linearizing an amplifier, the predistorter comprising a first set of circuitry adapted to generate a first high-order signal based on an input signal, wherein:

the first high-order signal is used to generate a predistorted input signal for application to the amplifier; and

the order of the first high-order signal is greater than or equal to five.

42. (new) The predistorter of claim 41, further comprising:

a second set of circuitry adapted to generate a second high-order signal based on the input signal, wherein:

the first and second high-order signals are used to generate the predistorted input signal; and

the order of the second high-order signal is greater than or equal to three and different from the order of the first high-order signal.

43. (new) The predistorter of claim 42, wherein the first and second high-order signals are odd-order signals.

44. (new) The predistorter of claim 43, wherein:
the first high-order signal is a fifth-order signal; and
the second high-order signal is a third-order signal.

45. (new) The predistorter of claim 44, further comprising a third set of circuitry adapted to generate a seventh-order signal.

46. (new) The predistorter of claim 43, wherein the first and second sets of circuitry are adapted to independently control the generation of the first and second high-order signals.

47. (new) The predistorter of claim 43, wherein the predistorter further comprises:
a variable phase-shift block and a variable attenuator block adapted to apply a selected phase shift and a selected attenuation level, respectively, to each of the first and second high-order signals;
a first summation node adapted to combine the phase-shifted, attenuated, first and second high-order signals to form a polynomial predistortion signal;
an amplifier adapted to amplify the polynomial predistortion signal; and
a second summation node adapted to combine the amplified, polynomial predistortion signal with the input signal to generate the predistorted input signal.

48. (new) The predistorter of claim 43, wherein:
the second high-order signal is a third-order signal; and
the second set of circuitry comprises:
a first combiner adapted to combine first and second versions of the input signal to generate a second-order signal;
a second combiner adapted to combine a third version of the input signal with the second-order signal to generate the third-order signal.

49. (new) The predistorter of claim 48, wherein the first and second combiners are mixers.

50. (new) The predistorter of claim 48, further comprising a controller adapted to inject a first DC signal during the generation of the third-order signal.

51. (new) The predistorter of claim 50, wherein the controller is adapted to generate the first DC signal to reduce input signal tone energy in the third-order signal.

52. (new) The predistorter of claim 50, wherein the controller is adapted to adaptively generate the first DC signal based on the input signal and the third-order signal.

53. (new) The predistorter of claim 52, wherein the controller comprises:
a mixer adapted to combine the input signal and the third-order signal to generate a mixer output signal; and
an integrator adapted to generate the first DC signal by integrating a signal based on the mixer output signal.

54. (new) The predistorter of claim 48, wherein the first high-order signal is a fifth-order signal.

55. (new) The predistorter of claim 54, wherein the first set of circuitry comprises a third combiner adapted to combine a version of the second-order signal with a version of the third-order signal to generate the fifth-order signal.

56. (new) The predistorter of claim 55, further comprising a controller adapted to inject a second DC signal during the generation of the fifth-order signal.

57. (new) The predistorter of claim 56, wherein the controller is adapted to generate the second DC signal to reduce third-order signal tone energy in the fifth-order signal.

58. (new) The predistorter of claim 56, wherein the controller is adapted to adaptively generate the second DC signal based on the third-order signal and the fifth-order signal.

59. (new) The predistorter of claim 54, wherein the first set of circuitry comprises:

a third combiner adapted to combine a third version of the input signal with the third-order signal to generate a fourth-order signal; and

a fourth combiner adapted to combine a fourth version of the input signal with the fourth-order signal to generate the fifth-order signal.

60. (new) The predistorter of claim 59, further comprising a controller adapted to inject a second DC signal during the generation of the fourth-order signal and a third DC signal during the generation of the fifth-order signal.

61. (new) The predistorter of claim 60, wherein the controller is adapted to generate the second and third DC signals to reduce third-order signal tone energy in the fifth-order signal.